EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 1
Spring 2020

Instructions: Students may bring 1 page of notes (front and back) to this exam. A scientific calculator will be provided but all personal electronic devices (smart phones, graphing calculators, ….) are not permitted. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/V^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0$. If reference to a diode is made, assume the process parameter $J_S=10^{-17}A/\mu^2$. The ratio of Boltzmann's constant to the charge of an electron is k/q= 8.61E-5 V/K. If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters

Short Answer Questions

1. (2pts) What is the approximate size of the SiO_2 molecule? Give the answer in angstroms (Å).

2. (2pts) One step in the photolithographic process is the “development” of the photoresist. What is the purpose of the “development” step?

3. (2pts) How many valence band electrons are in a silicon atom?

4. (2pts) What is the major difference between a diffused n-type region and an n-type epitaxial layer?

5. (2pts) When laying out transistors, a “dogbone” contact is often used to make contact to the gate. Why is the dogbone contact used?

6. (2 pts) Why is the capacitance density from Metal 2 to substrate smaller than the capacitance density from Metal 1 to substrate?

7. (2pts) It took a long time for the semiconductor industry to develop practical methods for forming copper interconnects. There were two major challenges that had to be overcome. Give one of the major challenges.

8. (2pts) When was the understanding of pn-junctions necessary to develop the "diode equation" first reported?

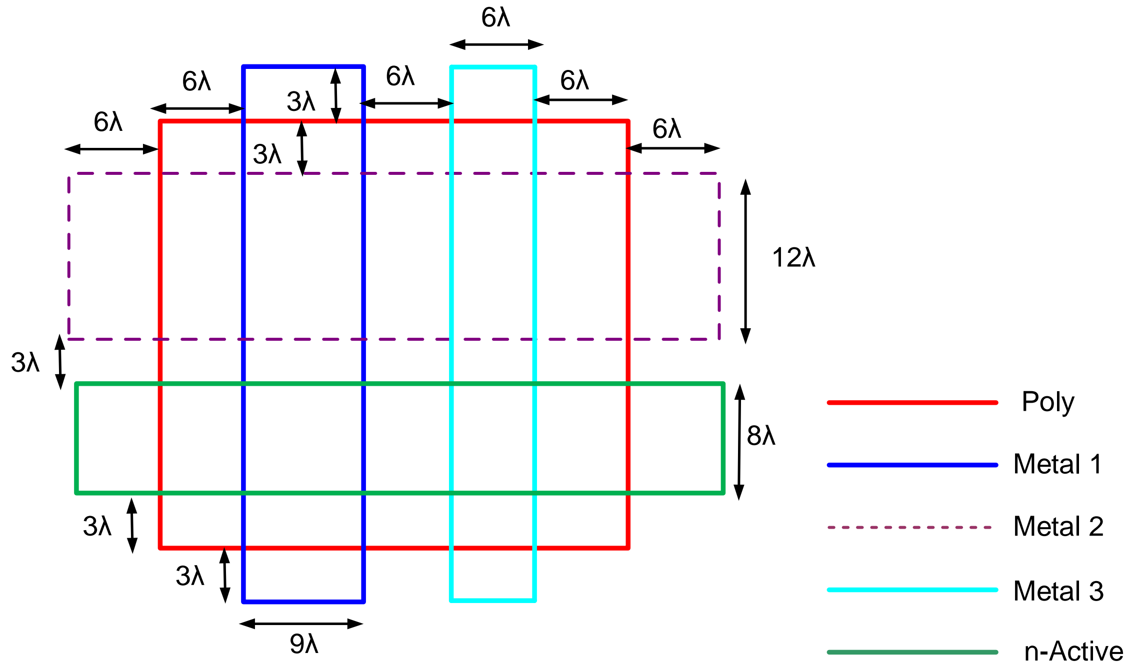
9. (2pts) When using STI (shallow trench isolation) to form a thick SiO_2 layer, is thermal growth or chemical vapor deposition used to create the SiO_2 layer?

10. (2pts) Since the mid 1950's, the major electronic device used for amplification has been either the MOSFET or the BJT. These are both referred to as transistors and the semiconductor industry has been in the "transistor era" since the mid 1950's. What was the major electronic device that was used for amplification for the three decades preceding emergence of the transistor era?

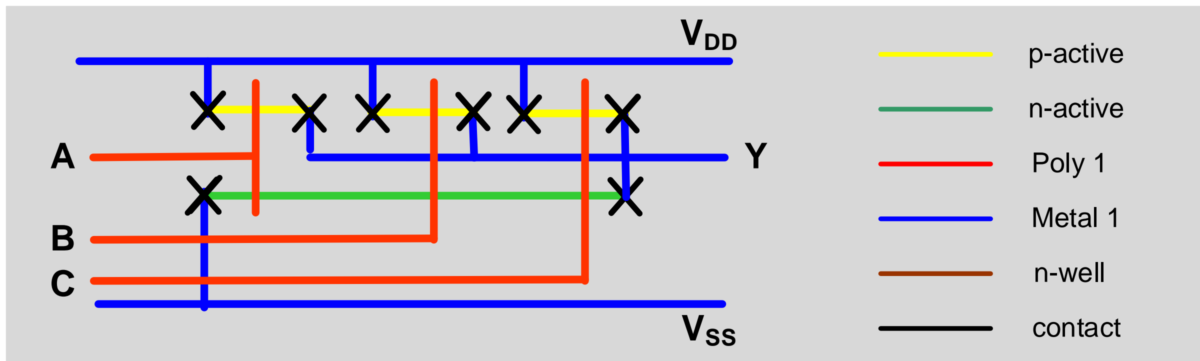
Problem 1 (16 pts)

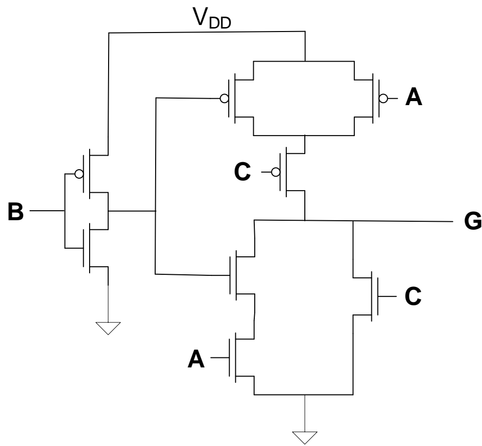
Five non-contacting regions are shown. Assume these features are fabricated in a 0.5μ CMOS process with $\lambda = 0.3\mu$.

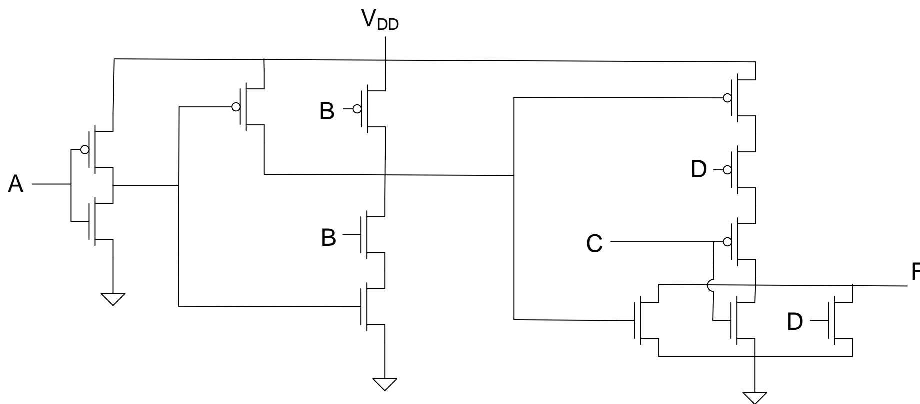
a) Determine the size of the transistor (i.e. W and L)
b) Determine the parasitic capacitance from Metal 1 to Metal 3
c) Determine the parasitic capacitance from Metal 1 to Metal 2
d) Determine the parasitic capacitance from Metal 2 to Substrate



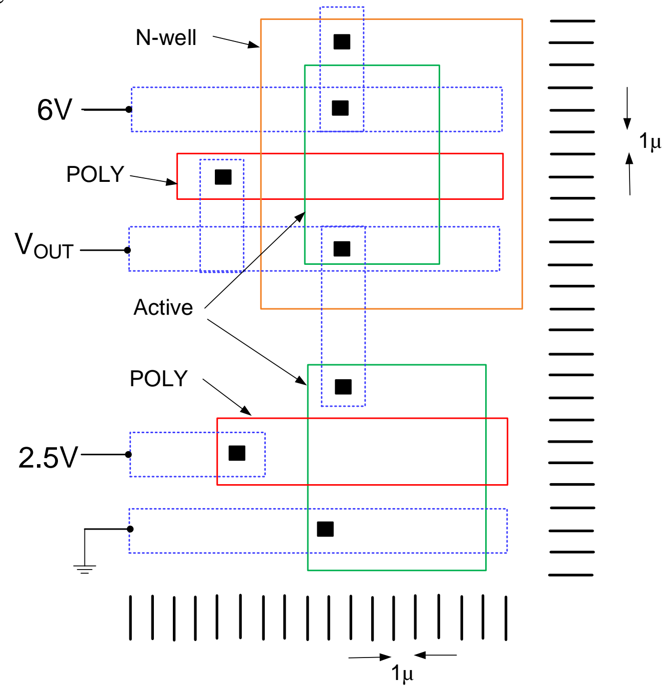
Problem 2 (16 pts)   Obtain expressions for the Boolean variables Y, F, and G.   Assume A, B, C, and D are Boolean inputs.







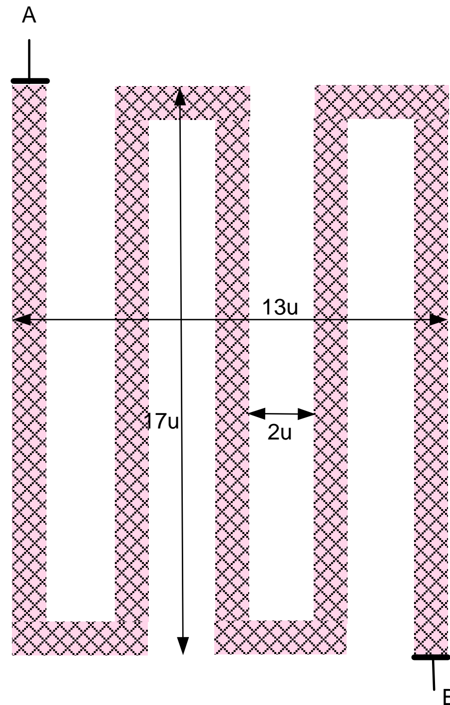
Problem 3 (16 pts) The layout of a simple circuit is shown below. Obtain the circuit schematic including device dimensions for all devices.



Problem 4 (16 pts) An n+ diffused resistor designed in a 0.5μ process is shown below where the individual traces in the resistor are all 1μm wide and where the two ends of the resistor are labeled as A and B in the figure. Assume the sheet resistance for the 0.5μ process is as given in the attached table where the given values are for operation at T=250K. Assume further that the TCR of the n+ diffused resistors are constant of value 1200 ppm/°C.

a) Determine the resistance between nodes A and B at T=250K.

b) What will be the resistance at T=300°K?



Problem 5 (16 pts) Assume the cost of 12” wafers in a CMOS process is $1200 and the defect density is $1.2/cm^2$. If the cost per good die on a project must not exceed $1.50, what is the maximum area that can be used for the die? Assume a 100% soft yield.

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU | VENDOR: AMIS
TECHNOLOGY: SCN05 | FEATURE SIZE: 0.5µm
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	**83.5**	**105.3**	**23.5**	**999**	**44.2**	**0.09**	**0.10**	ohms/sq
Contact Resistance	**64.9**	**149.7**	**17.3**		**29.2**		**0.97**	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	**0.05**	**824**	**816**	ohms/sq
Contact Resistance	**0.79**			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	**425**	**731**	**84**		**27**	**12**	**7**	**37**	aF/um^2
Area (N+active)			**2434**		**35**	**16**	**11**		aF/um^2
Area (P+active)			**2335**						aF/um^2
Area (poly)				**938**	**56**	**15**	**9**		aF/um^2
Area (poly2)					**49**				aF/um^2
Area (metal1)						**31**	**13**		aF/um^2
Area (metal2)							**35**		aF/um^2
Fringe (substrate)	**344**	**238**			**49**	**33**	**23**		aF/um
Fringe (poly)					**59**	**38**	**28**		aF/um
Fringe (metal1)						**51**	**34**		aF/um
Fringe (metal2)							**52**		aF/um
Overlap (N+active)			**232**						aF/um
Overlap (P+active)			**312**						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate